B5 A3 Cont.

and

exposing the memory cell to an atmosphere that comprises Hydrogen isotope.

Sub B6 A4

37. (Amended) A method for overlaying source and drain regions of a non-volatile, electrically alterable semiconductor memory cell with a thermal oxide layer thereby reducing random, single bit data loss in a memory circuit, comprising:

providing a silicon substrate;

defining source and drain regions; and

growing the thermal oxide layer over the source and drain regions in an atmosphere that comprises Hydrogen isotope.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on November 3, 2000, and the references cited therewith.

Claims 6, 26, 35, and 37 are amended. Claims 1-14, 26-32, and 35-39 are pending in this application.

§112 Rejection of the Claims

Claim 6 was rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Applicant has amended claim 6 to describe a semiconductor "layer." It is believed that the claim in a condition for allowance. It is respectfully requested that the Examiner reconsider and withdraw the rejection.

§103 Rejection of the Claims

Claims 1-14, 26-32, and 35-38 have been rejected under 35 USC § 103(a) as being unpatentable over Lisenker et al. (PCT/WO 94-19829). The Examiner acknowledges that the Lisenker et al. reference does not anticipate the processes claimed herein. The Examiner also acknowledges that the Lisenker et al reference does not refer to or describe FLASH devices. The